Jesús G. Stiles Amezcua

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EDUCATION

B.S. Electrical & Computer Engineering — Expected May 2027
A.S. Engineering Science, Middlesex College, Edison, NJ — Expected May 2026

TECHNICAL EXPERIENCE

Languages: C, C++, Java, Verilog, MATLAB, Python, HTML/CSS/JS
Hardware: Artix-7/Basys-3 FPGA; ESP32/Arduino; PCB design; scopes, DMMs; soldering
Tools/Focus: Vivado, Arduino IDE, PyTorch, Git, CAD, UART, REST APIs; Digital Design, Embedded Systems, ESP-NOW, IoT

EXPERIENCE

Hardware Engineering Intern
Warcola Honey Farms, Redwood, NY | June 2025 - August 2025

- Delivered reliable 24/7 honey production monitoring system serving 3 remote tanks with <0.1% packet loss over 2-month deployment with zero system failures in harsh outdoor conditions
- Architected distributed 5-MCU ESP32 system using ESP-NOW wireless protocol with 120-second deep sleep cycles for extended battery life achieving 1.5+ months on a single battery pack.
- Resolved critical wireless reliability issues through systematic debugging: channel scanning, power optimization, and custom CRC-8 validation reducing packet retry rate from 15% to <0.1%

Consultant Agent
Geek Squad, Best Buy, Woodbridge, NJ | May 2024 – November 2024

- Achieved 95% first-visit resolution rate while diagnosing 15+ devices weekly, saving customers average 3-day turnaround time
- Performed component-level troubleshooting including RAM/SSD upgrades, PSU testing, and motherboard diagnostics using test benches and specialized diagnostic software
- Translated complex technical failures into actionable solutions for 50+ non-technical clients weekly

TECHNICAL PROJECTS

FPGA Mini-GPU with VGA Output | *Current Personal Project* | Sept 2024 - Present
Technologies: Verilog, Python, UART, Artix-7 FPGA

- Demonstrating real-time graphics performance with interactive games (Pong, Snake) rendered entirely in FPGA hardware logic
- Designing custom 2D graphics pipeline on Artix-7 FPGA supporting 640×480@60Hz VGA output with 12-bit RGB color and 25MHz pixel clock timing
- Implementing dual-port BRAM architecture with double buffering, achieving tear-free rendering in <225KB memory footprint
- Developing Python host toolchain for streaming images/sprites via UART and GPU-like raster functions (Bresenham line drawing, tilemap rendering) with collision detection

Real-Time Agricultural Environmental Monitor | *IoT System* | June 2024
[github.com/stilesjesus/potato-sensor-esp32] | **Technologies:** ESP32, DHT22, REST API, WebServer, ArduinoJson

- Delivered near-real-time temperature/humidity monitoring system critical for preventing crop loss in storage facilities
- Implemented dual-interface architecture with 1.5" OLED display and mobile-responsive web dashboard featuring live JSON/REST endpoints for data integration
- Engineered non-blocking event loop co-hosting HTTP server and sensor sampling with NTP-synchronized timestamps for data integrity with <50ms server response time
- Developed 4-phase pixel-shift algorithm preventing OLED burn-in and automatic min/max aggregation

LEADERSHIP & ACHIEVEMENTS

First Place, NSBE Regional Elevator Pitch Competition | March 2024

- Presented innovative automated bathroom fan system designed for accessibility and disability assistance

Eagle Scout Award | Boy Scouts of America | 2022

- Led environmental restoration project reintroducing native wildlife species to flood zone, preventing future erosion

Member, Society of Hispanic Professional Engineers (SHPE) | 2024 – Present
Member, National Society of Black Engineers (NSBE) | 2024 – Present

ADDITIONAL INFORMATION

Bilingual: English/Spanish • **US citizen (**clearance-eligible**) • Interests:** RL (PyTorch bipedal walker), DSP, 3D printing